WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a silicon layer having a first diffused region and a second diffused region formed therein;

a gate electrode formed through an insulating film on one side of the silicon layer between the first and the second diffused regions;

a capacitor formed on said one side of the silicon layer and having a storage electrode connected to the first diffused region; and

a bit line formed on the other side of the silicon layer and connected to the second diffused region.

2. A semiconductor memory device comprising:

a silicon layer having a first diffused region and a second diffused region formed therein;

a gate electrode formed through an insulating film on one side of the silicon layer between the first and the second diffused regions;

a capacitor formed on said one side of the silicon layer and having a storage electrode connected to the first diffused region;

a bit line formed on said one side of the silicon layer and connected to the second diffused region; and

a scrapping word line formed on the other side of the silicon layer and connected to the gate electrode.

3. A semiconductor memory device according to claim

1, wherein

a connection surface of the storage electrode, which are connected to the first diffused region, is substantially parallel with a surface of the storage electrode, which correspond to the connection surface.

4. A semiconductor memory device according to claim 2, wherein

a connection surface of the storage electrode, which are connected to the first diffused region, is substantially parallel with a surface of the storage electrode, which correspond to the connection surface.

5. A semiconductor memory device comprising:

a device layer including a semiconductor layer having a first diffused region and a second diffused region formed therein, a transistor having a gate electrode formed through an insulation film on one side of the semiconductor layer between the first and the second diffused regions, and a capacitor formed on said one side of the semiconductor layer and having a storage electrode connected to the first diffused region;

a bit line formed on the other side of the semiconductor layer, and extended in a direction normal to the gate electrode; and

a support substrate formed on said one side of the semiconductor layer for supporting the device layer;

the semiconductor layer including a first region which

is extended in the direction of extension of the bit line and includes the first diffused region and the second diffused region, and a second region which is extended in a direction of extension of the gate electrode in the first region and includes the second diffused region;

a first contact hole being formed in the first region for connecting the first diffused region to the capacitor; and

a second contact hole being formed in the second region for connecting the bit line with the second diffused region.

6. A semiconductor memory device according to claim 5, wherein

the first region and the second region are connected with each other.

7. A semiconductor memory device according to claim 5, wherein

the second diffused region in the first region and the second diffused region in the second region are formed spaced from each other.

8. A semiconductor memory device according to claim 6, further comprising

a first wiring layer formed on said one side of the semiconductor layer for connecting the first and the second regions with each other.

9. A semiconductor memory device according to claim

7, further comprising

a first wiring layer formed on said one side of the semiconductor layer for connecting the first and the second regions with each other.

10. A semiconductor memory device according to claim 5, further comprising

a scrapping word line formed on said other side of the semiconductor layer and connected to the gate electrode.

11. A semiconductor memory device according to claim 5, further comprising

a scrapping word line formed on said one side of the semiconductor layer and connected to the gate electrode.

12. A semiconductor memory device according to claim 5, further comprising

a shield electrode formed on the bit line for suppressing interference between the bit lines.

13. A semiconductor memory device according to claim 5, further comprising

a second wiring layer formed on said the other side of the semiconductor layer and electrically connected to a region of the semiconductor layer between the first and the second diffused regions.

14. A semiconductor memory device according to claim 5, wherein

the bit line is electrically connected to a region of the semiconductor layer between the first and the second

diffused regions.

15. A method for fabricating a semiconductor memory device comprising:

a gate electrode forming step of forming a gate electrode on one side of a semiconductor substrate;

a diffused region forming step of implanting an impurity into the semiconductor substrate with the gate electrode as a mask to form a first diffused region and a second diffused region;

a capacitor forming step of forming a capacitor having a storage electrode connected to the first diffused region on the semiconductor substrate with the first and the second diffused regions formed therein;

a support substrate forming step of forming a support substrate on the semiconductor substrate with the capacitor formed thereon; and

a semiconductor layer forming step of removing the semiconductor substrate at the other side of the semiconductor substrate until bottoms of the second and the first diffused regions are exposed, to form a semiconductor layer.

16. A method for fabricating a semiconductor memory device according to claim 15, further comprising, after the semiconductor layer forming step, a bit line forming step of forming a bit line connected to the second diffused region.

17. A method for fabricating a semiconductor memory device according to claim 16, further comprising, after the bit line forming step, a shield electrode forming step of forming a shield electrode for suppressing interference between the bit lines.

18. A method for fabricating a semiconductor memory device according to claim 16, further comprising, after the diffused region forming step and before the bit line forming step, a wiring layer forming step of forming a wiring layer for reducing connection resistance between the bit line and the second diffused region.

19. A method for fabricating a semiconductor memory device according to claim 15, further comprising, after the diffused region forming step and before the support substrate forming step, a bit line forming step of forming a bit line connected to the second diffused region.

20. A method for fabricating a semiconductor memory device according to claim 15, further comprising, after the semiconductor layer forming step, a scrapping word line forming step of forming a scrapping word line connected to the gate electrode.

21. A method for forming a semiconductor memory device according to claim 15, further comprising, after the diffused region forming step, a scrapping word line forming step of forming a scrapping word line connected to the gate electrode.

22. A method for fabricating a semiconductor memory device according to claim 15, wherein

after the semiconductor layer forming step, the semiconductor layer except the device region is removed.

23. A method for fabricating a semiconductor memory device according to claim 15, wherein

after the semiconductor layer forming step, an impurity of a conduction type different from that of the second and the first diffused regions is doped in a region of the semiconductor layer where no active element is formed.

24. A method for fabricating a semiconductor memory device according to claim 15, wherein

the method further comprises, before the gate electrode forming step, a device isolation film forming step of forming on said one side of the semiconductor substrate a device isolation film which defines a device region; and

in the semiconductor layer forming step the semiconductor substrate is removed at said other side of the semiconductor substrate until a bottom of the device isolation film is exposed.

25. A method for fabricating a semiconductor memory device according to claim 16, wherein

the method further comprises, before the gate electrode forming step, a device isolation film forming

step of forming on said one side of the semiconductor substrate a device isolation film which defines a device region;

in the device isolation film forming step, the device region including a first region which is extended in a direction of extension of the bit line and includes the first and the second diffused regions, and a second region which is extended in a direction of extension of the gate electrode in the first region and includes the second diffused region, is formed;

in the capacitor forming step the first diffused region is connected with the capacitor in the first region;

in the semiconductor forming step the semiconductor substrate is removed at said other side of the semiconductor substrate until a bottom of the device isolation film is exposed; and

in the bit line forming step the bit line is connected with the second diffused region in the second region.

26. A method for fabricating a semiconductor memory device according to claim 18, wherein

the method further comprises, before the gate electrode forming step, a device isolation film forming step of forming on said one side of the semiconductor substrate a device isolation film which defines a device region;

in the device isolation film forming step, the device

region including a first region which is extended in a direction of extension of the bit line and includes the first and the second diffused regions, and a second region which is extended in a direction of extension of the gate electrode in the first region and includes the second diffused region, is formed;

in the capacitor forming step the first diffused region is connected with the capacitor in the first region;

in the semiconductor forming step the semiconductor substrate is removed at said other side of the semiconductor substrate until a bottom of the device isolation film is exposed; and

in the bit line forming step the bit line is connected with the second diffused region in the second region.

27. A method for fabricating a semiconductor memory device according to claim 15, wherein

the method further comprises, before the gate electrode forming step, a device isolation film forming step of forming on said one side of the semiconductor substrate a device isolation film which defines a device region, and a opening forming step of removing the device isolation film in the first region of the device isolation film to form an opening;

the method further comprises, after the semiconductor layer forming step, a scrapping word line forming step of forming a scrapping word line connected to the gate

electrode;

in the gate electrode forming step the gate electrode extended in the first region is formed buried in the opening; and

in the scrapping word line forming step the scrapping word line is connected with the gate electrode in the first region.

28. A method for fabricating a semiconductor memory device comprising a device isolation film forming step of forming a device isolation film on one side of a semiconductor layer, a semiconductor device forming step of forming a semiconductor device on the semiconductor substrate with the device isolation film formed on, and a semiconductor layer forming step of forming a semiconductor layer,

in a case that the device isolation film includes a first device isolation film having a first film thickness and a second device isolation film having a second film thickness which is smaller than the first film thickness, the semiconductor layer forming step comprising the steps of

polishing the semiconductor substrate until the first device isolation film is exposed,

etching the exposed first device isolation film so that the first device isolation film and the second device isolation film have substantially the same film thickness,

and

polishing the semiconductor substrate until the second device isolation film is exposed.